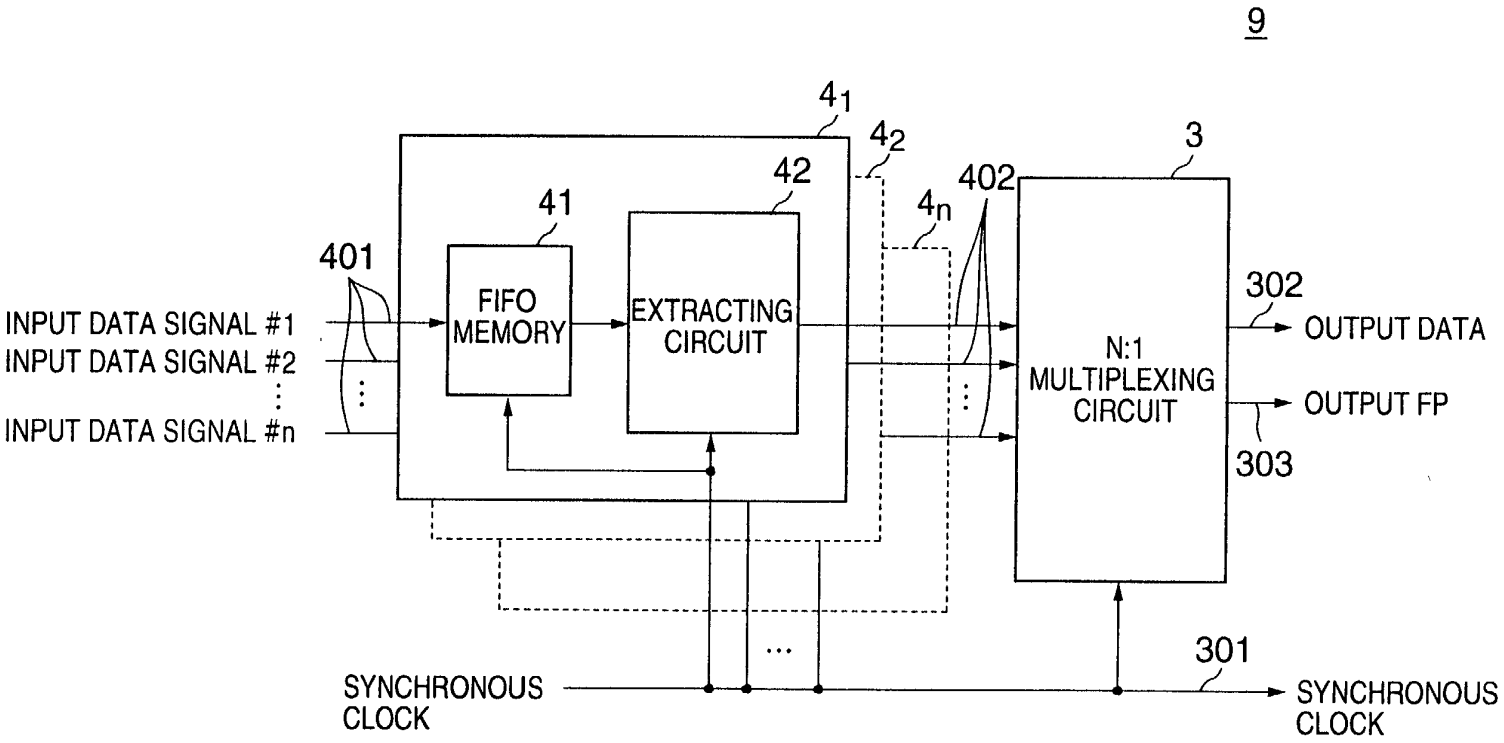

FIG.1 PRIOR ART

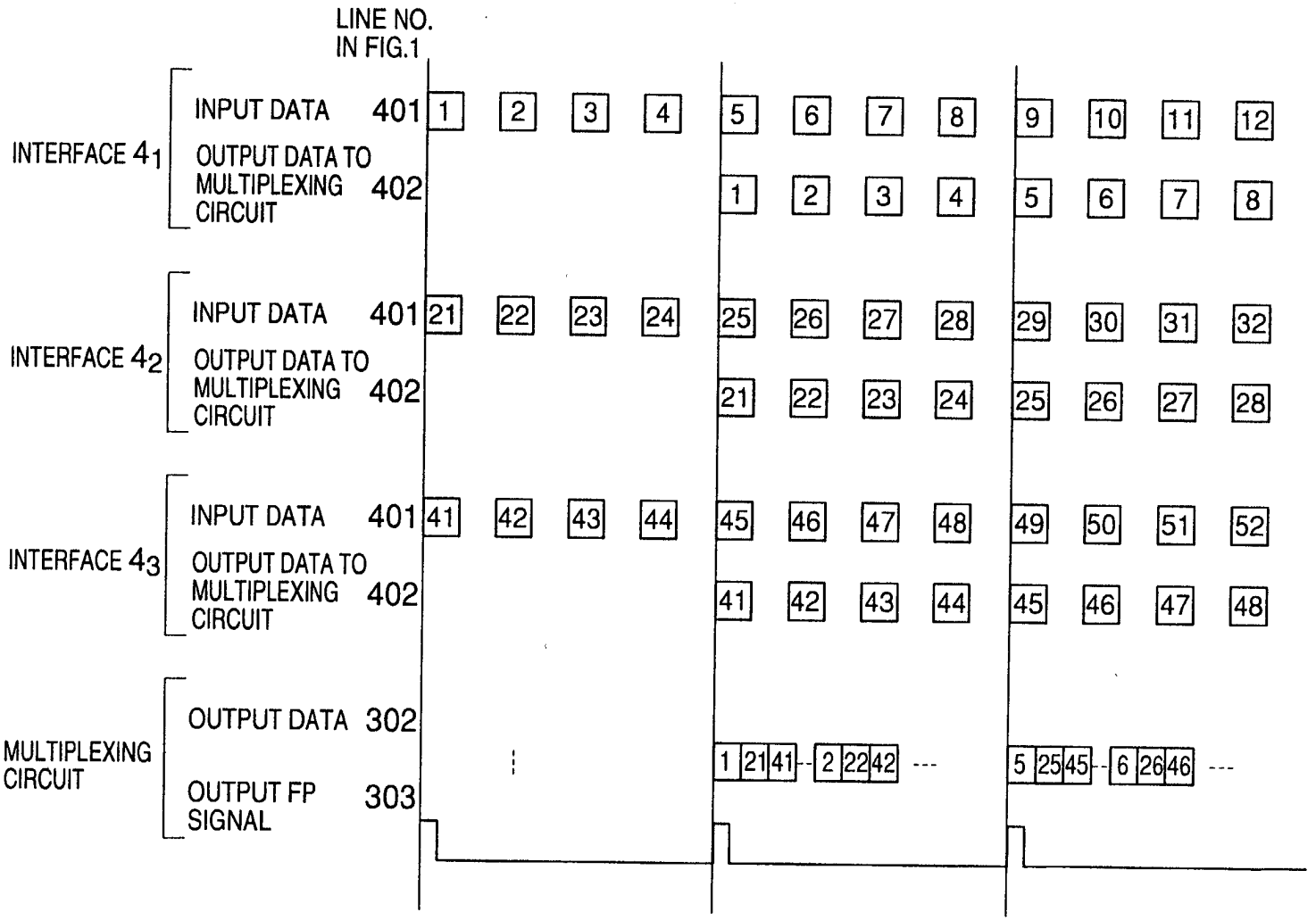

FIG.2 PRIOR ART

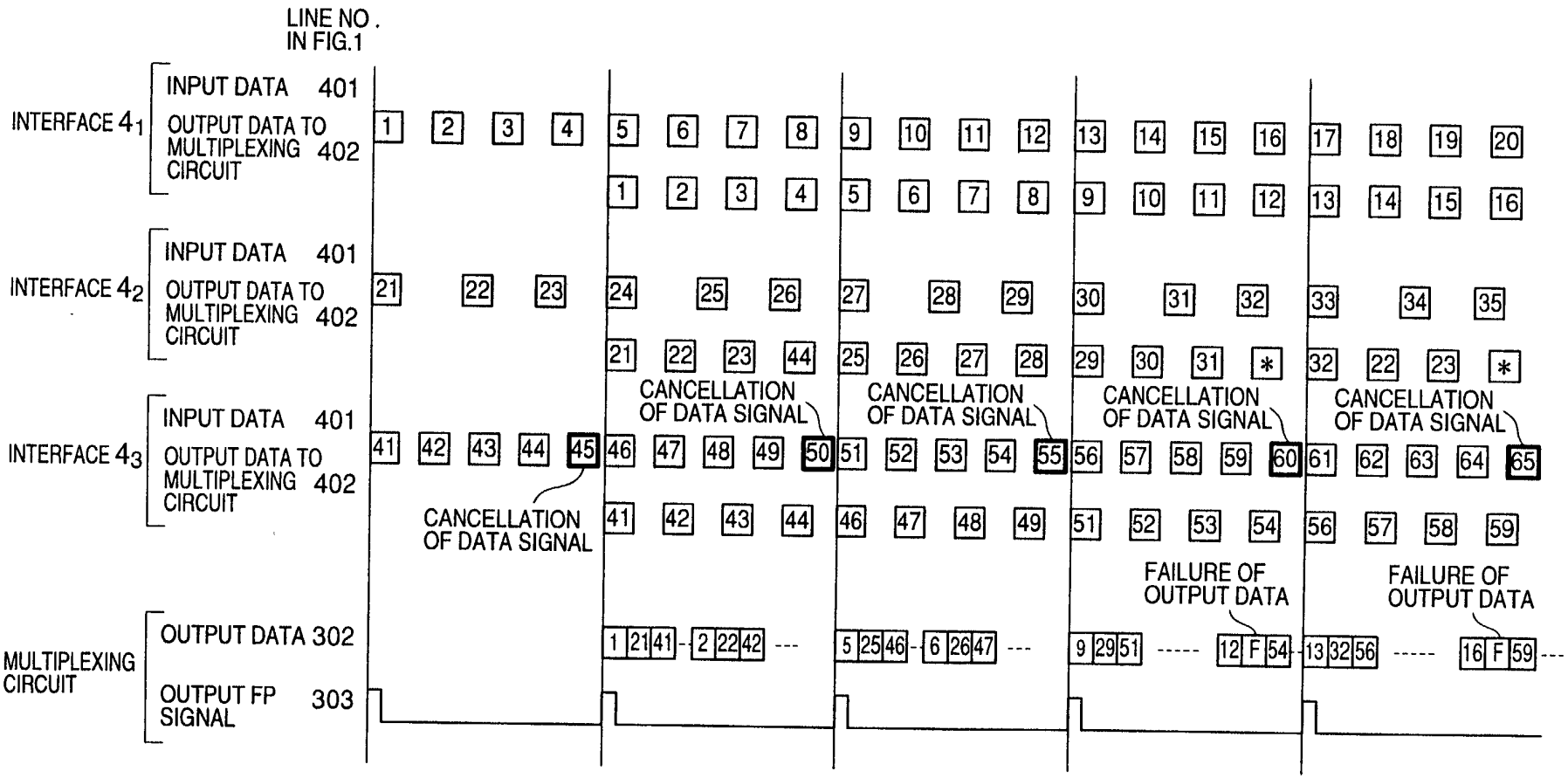

FIG.3 PRIOR ART

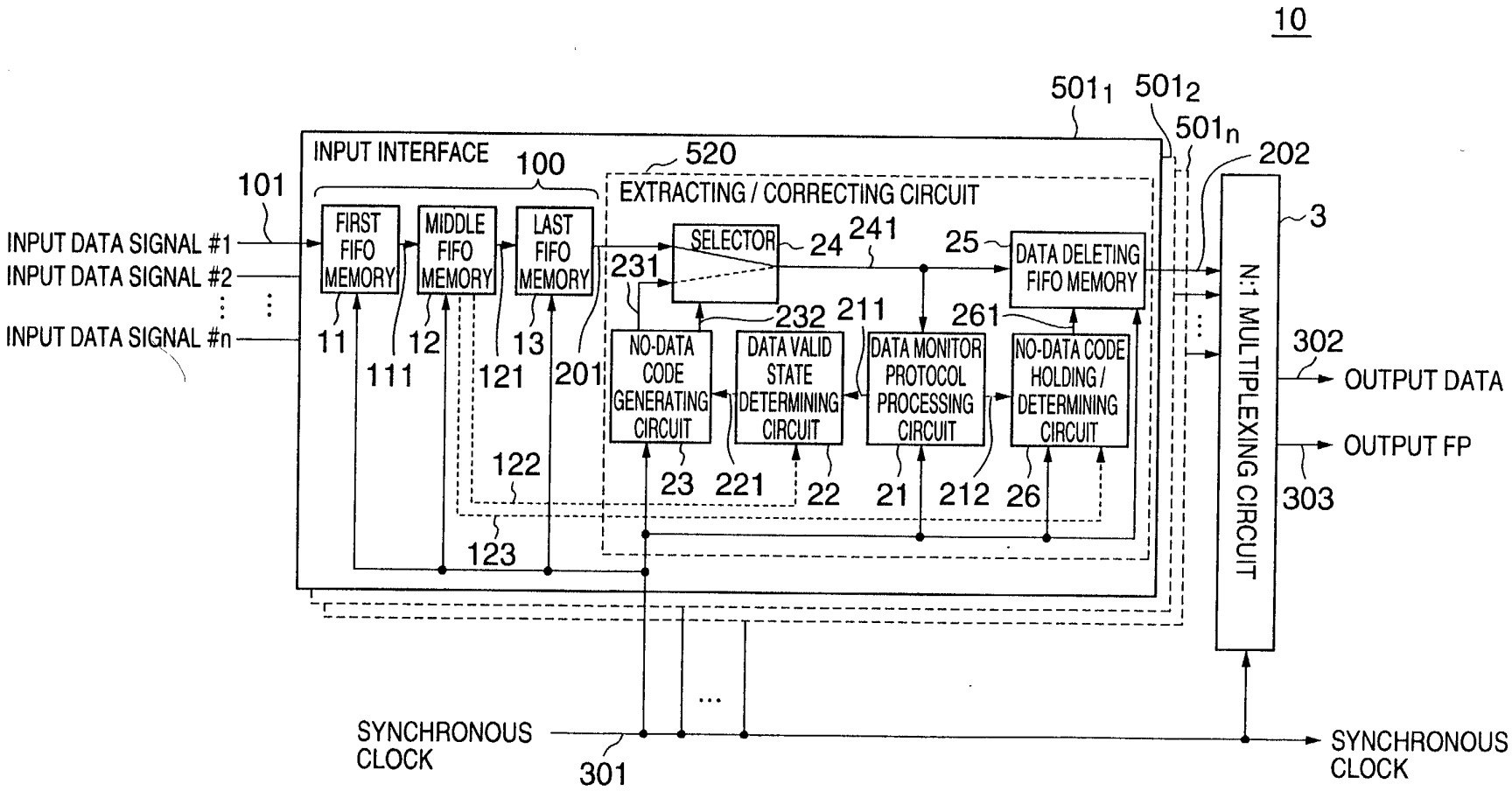

FIG.4

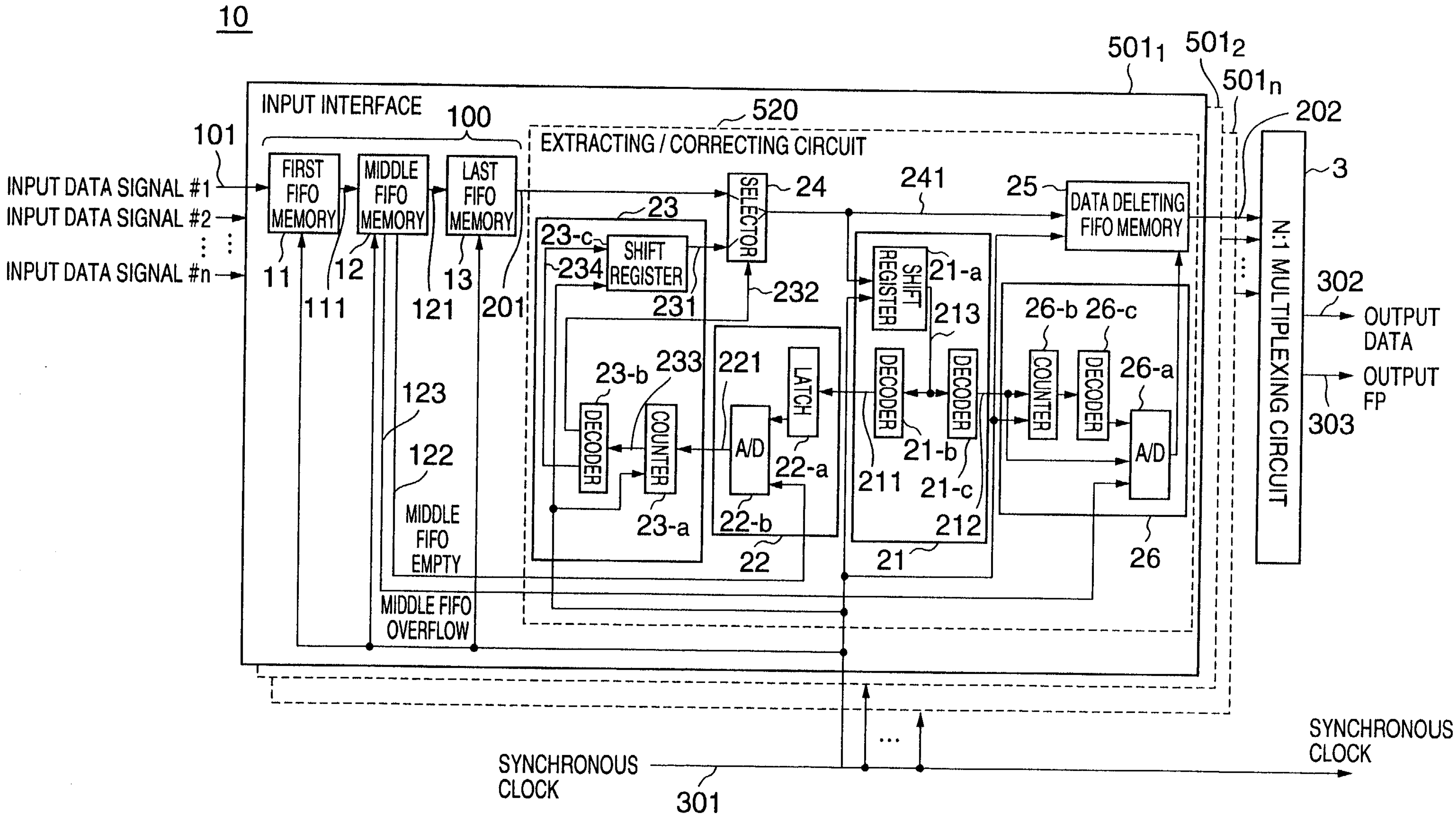
10
INPUT DATA SIGNAL #1
INPUT DATA SIGNAL #2
INPUT DATA SIGNAL #n
101
INPUT INTERFACE
100
FIRST FIFO MEMORY
MIDDLE FIFO MEMORY
LAST FIFO MEMORY
11
111
12
121
13
201
123
122
MIDDLE FIFO EMPTY
MIDDLE FIFO OVERFLOW
520
EXTRACTING / CORRECTING CIRCUIT
23
23-c
234
SHIFT REGISTER
231
23-b
233
DECODER
COUNTER
23-a
SELECTOR
24
232
221
LATCH
A/D
22-a
22-b
22
241
SHIFT REGISTER
21-a
213
DECODER
DECODER
21-b
211
21-c
212
21
25
DATA DELETING FIFO MEMORY
26-b 26-c
COUNTER
DECODER
26-a
A/D
26
501₁
501₂
501ₙ
202
3
N:1 MULTIPLEXING CIRCUIT
302
OUTPUT DATA
OUTPUT FP
303
SYNCHRONOUS CLOCK
301
SYNCHRONOUS CLOCK

FIG.5

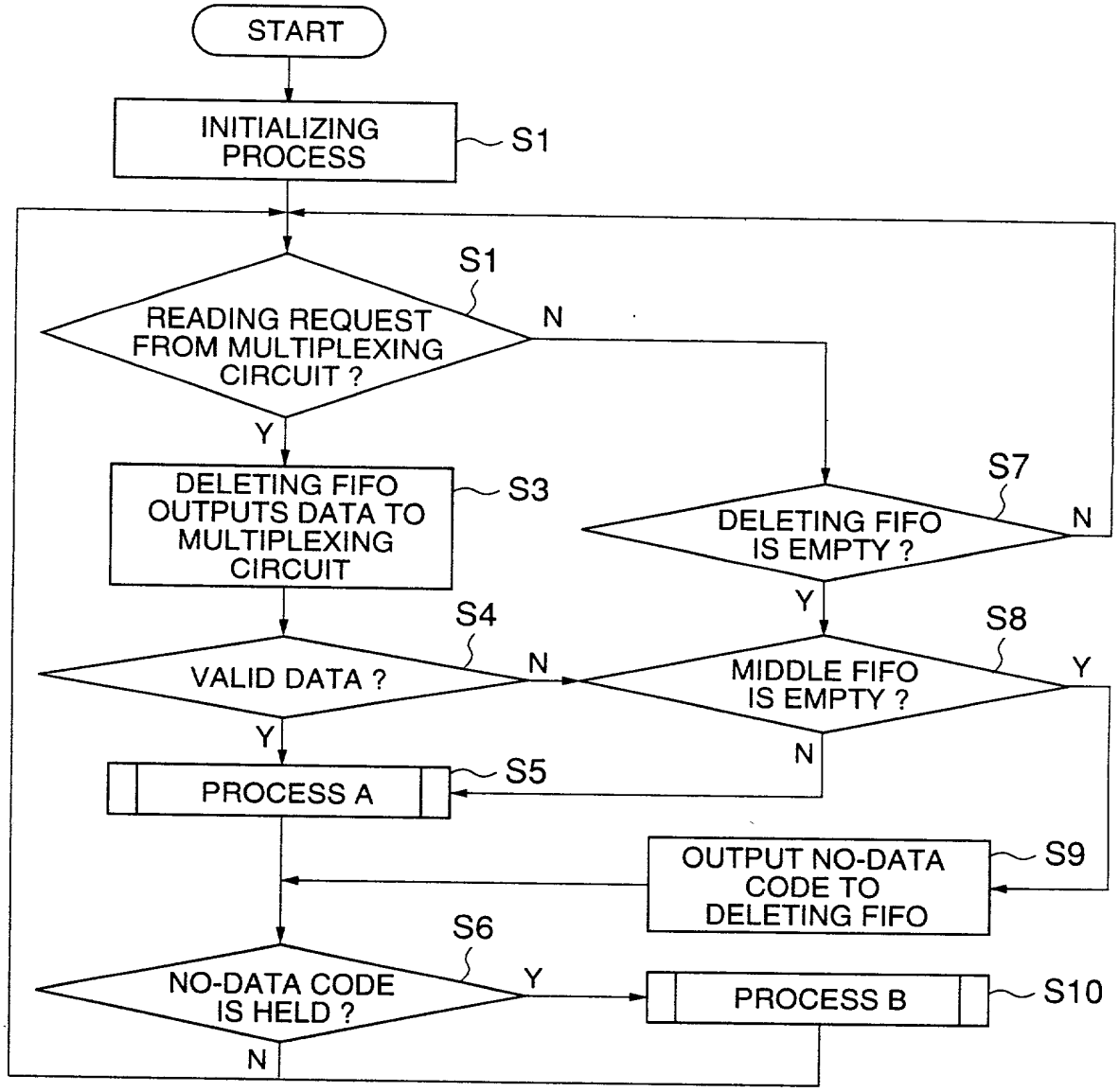

FIG.6

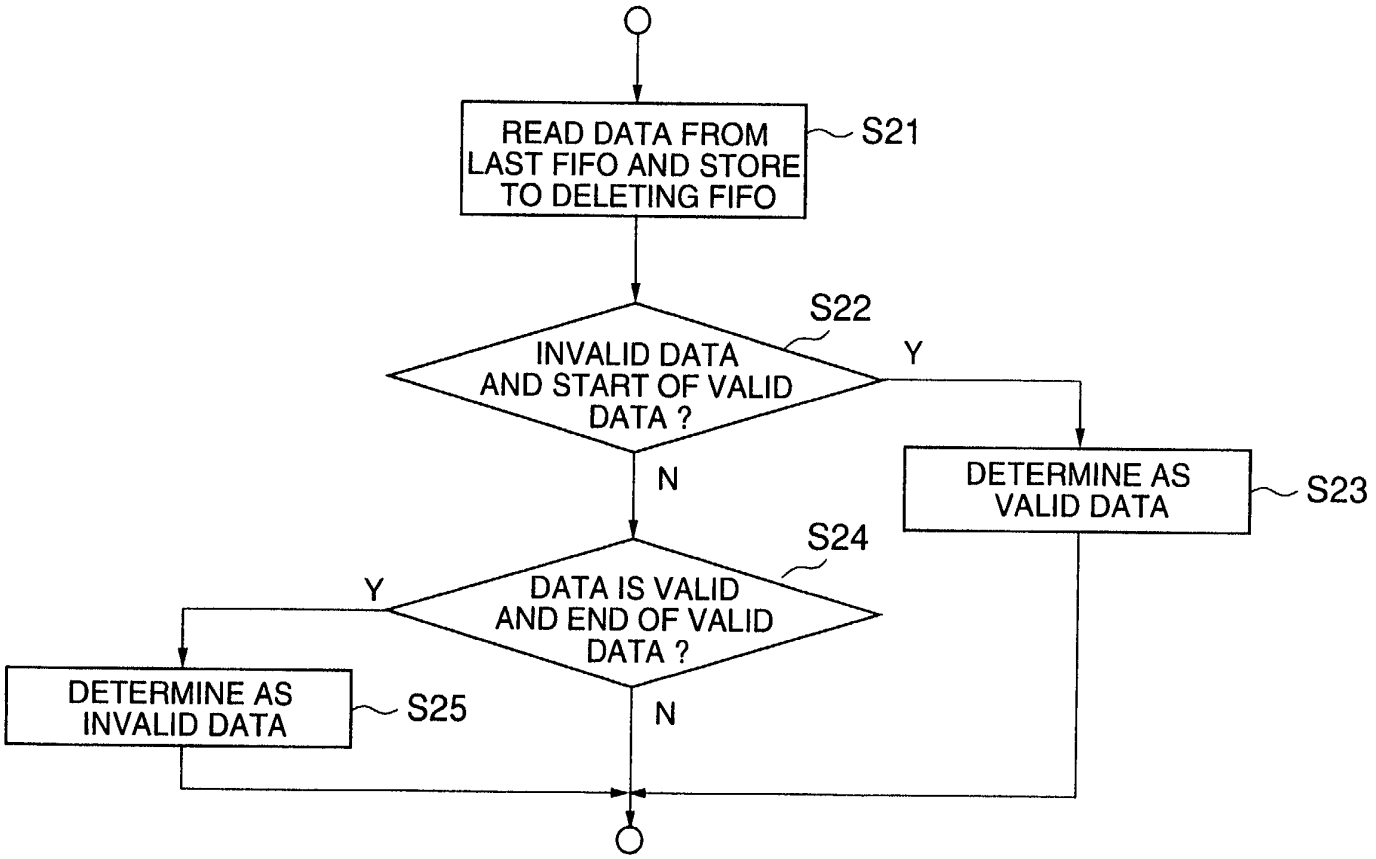
READ DATA FROM LAST FIFO AND STORE TO DELETING FIFO
S21
S22
INVALID DATA AND START OF VALID DATA ?
Y
N
DETERMINE AS VALID DATA
S23
S24
Y
DATA IS VALID AND END OF VALID DATA ?
DETERMINE AS INVALID DATA
S25
N

FIG.7

FIG.8

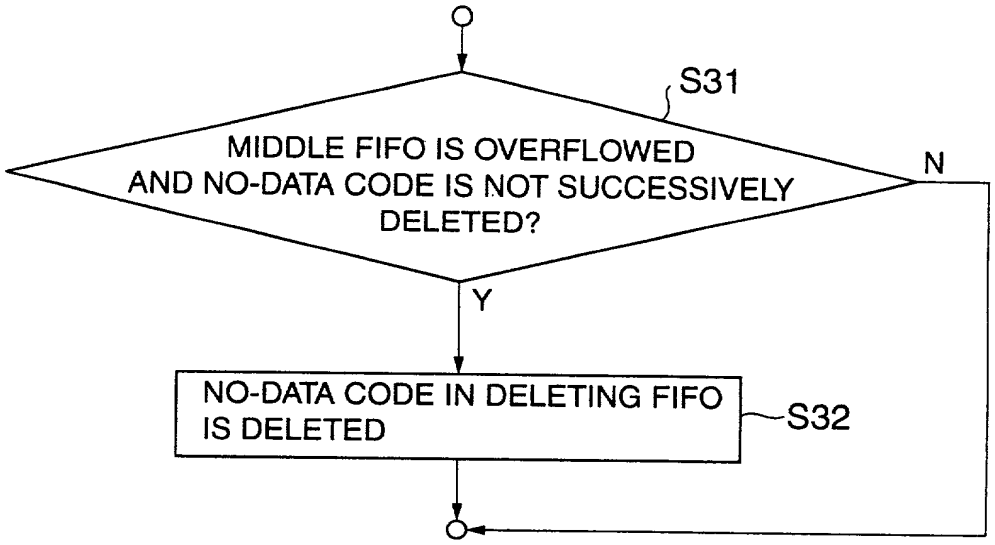
S31
MIDDLE FIFO IS OVERFLOWED AND NO-DATA CODE IS NOT SUCCESSIVELY DELETED?
N
Y
NO-DATA CODE IN DELETING FIFO IS DELETED
S32

FIG.9

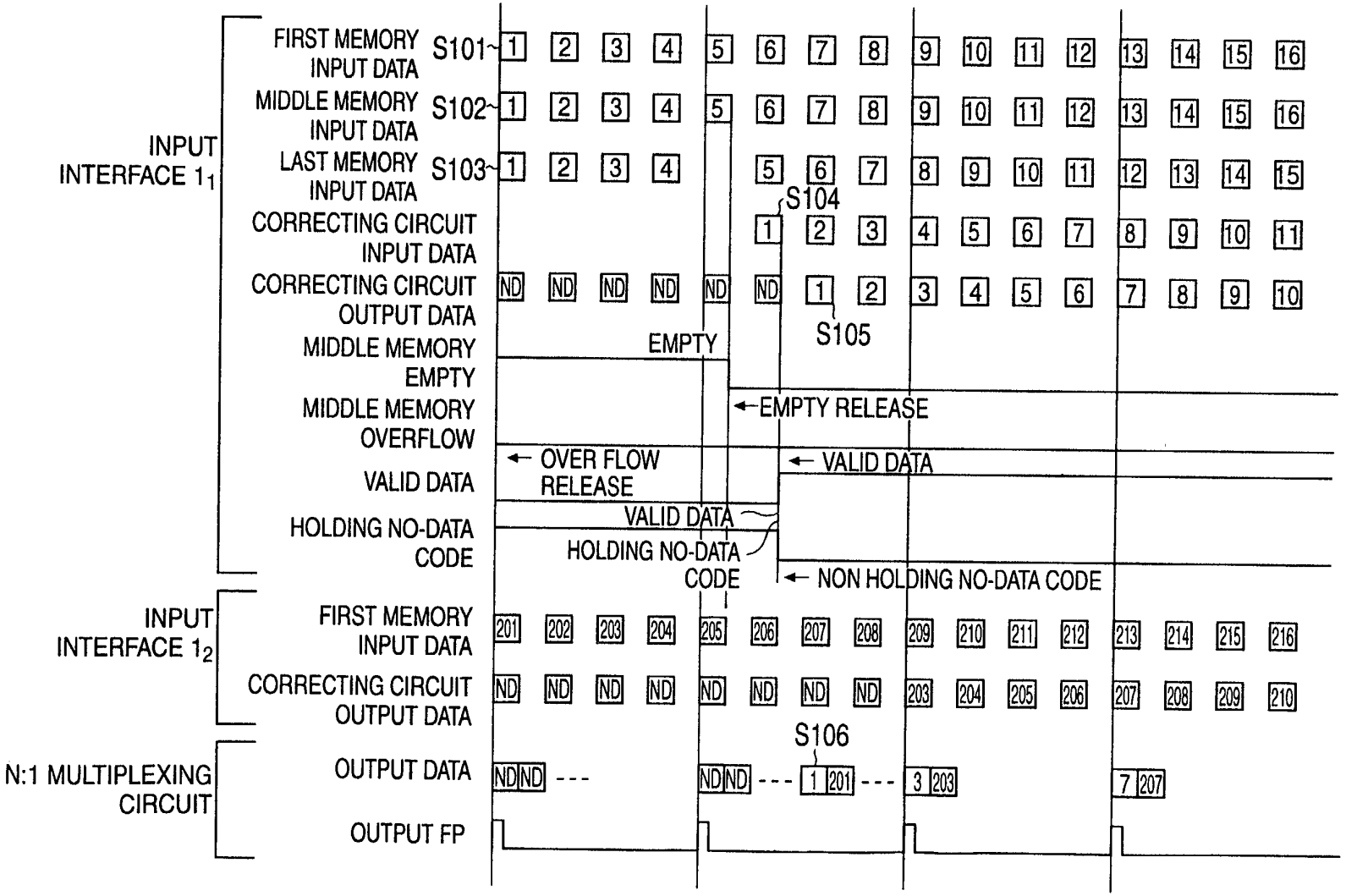

FIG.10

INPUT DATA	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
MIDDLE FIFO MEMORY					5	6	7	8	9	10	11	12	13	14	15	16
LAST FIFO MEMORY	S103 ①	2 1	3 2 1	4 3 2 1	4 3 2 1	5 4 3 2	6 5 4 3	7 6 5 4	8 7 6 5	9 8 7 6	10 9 8 7	11 10 9 8	12 11 10 9	13 12 11 10	14 13 12 11	15 14 13 12
CIRCUIT INPUT	0	0	0	0	0	①	2	3	4	5	6	7	8	9	10	11
CIRCUIT OUTPUT	0	0	0	0	0	0	①	2	3	4	5	6	7	8	9	10
					S104		S105									
EMPTY	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
VALID DATA	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

FIG.11

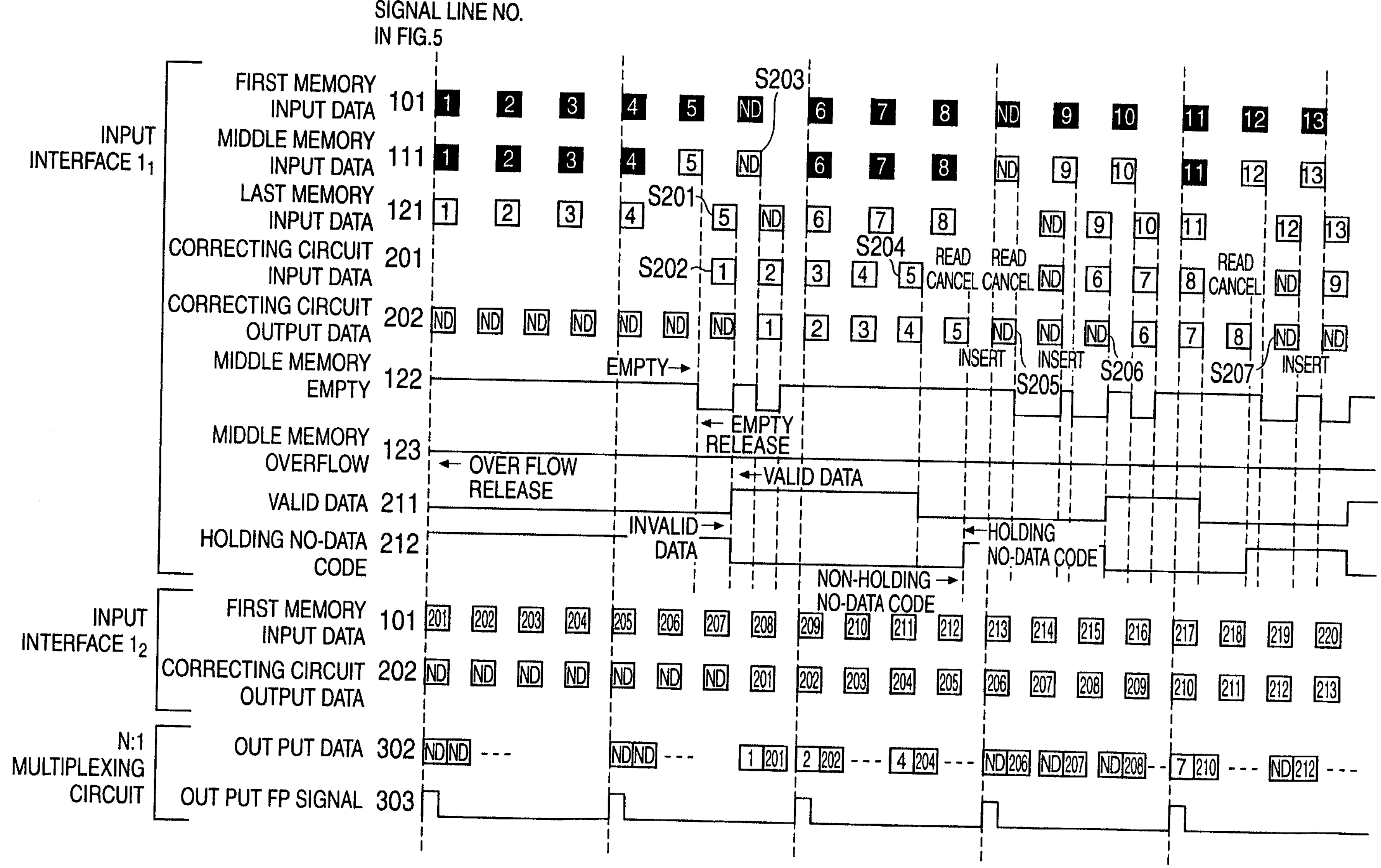
SIGNAL LINE NO.
IN FIG.5
INPUT
INTERFACE 1_1
FIRST MEMORY
INPUT DATA 101
MIDDLE MEMORY
INPUT DATA 111
LAST MEMORY
INPUT DATA 121
CORRECTING CIRCUIT
INPUT DATA 201
CORRECTING CIRCUIT
OUTPUT DATA 202
MIDDLE MEMORY
EMPTY 122
MIDDLE MEMORY
OVERFLOW 123
VALID DATA 211
HOLDING NO-DATA
CODE 212
INPUT
INTERFACE 1_2
FIRST MEMORY
INPUT DATA 101
CORRECTING CIRCUIT
OUTPUT DATA 202
N:1
MULTIPLEXING
CIRCUIT
OUT PUT DATA 302
OUT PUT FP SIGNAL 303
S201
S202
S203
S204
S205
S206
S207
READ CANCEL
INSERT
EMPTY
EMPTY RELEASE
OVER FLOW RELEASE
VALID DATA
INVALID DATA
HOLDING NO-DATA CODE
NON-HOLDING NO-DATA CODE

FIG.12

INPUT DATA	1		2	3	4		5		IC		6		7		8		IC		9		10		11		12		13	
MIDDLE FIFO MEMORY							5		(IC)								IC		9		10				12		13	
LAST FIFO MEMORY	1	1	2 1	3 2 1	4 3 2 1	4 3 2 1	4 3 2 1	(5) 4 3 2	5 4 3 2	IC 5 4 3	8 IC 5 4	6 IC 5	7 6 IC 5	7 6 IC	8 7 6 IC	8 7 6 IC	8 7 6 IC	IC 8 7 6	IC 8 7 6	9 IC 8 7	9 IC 8 7	10 9 IC 8	11 10 9 IC	11 10 9 IC	11 10 9 IC	12 11 10 9	12 11 10 9	13 12 11 10
CIRCUIT INPUT	0	0	0	0	0	0		(1)		2	3	4		(5)		(0)	(0)	IC		6		7	8	(0)		IC		9
CIRCUIT OUTPUT	0	0	0	0	0	0		0		1	2	3		4		5	0	0		IC		6	7	8		0		IC
EMPTY	1	1	1	1	1	1	1	0	1	0	1	1	1	1	1	1	1	0	1	0	1	0	1	1	1	0	1	0
VALID DATA	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0

S201, S202, S203, S204, S205, S206, S207

FIG.13

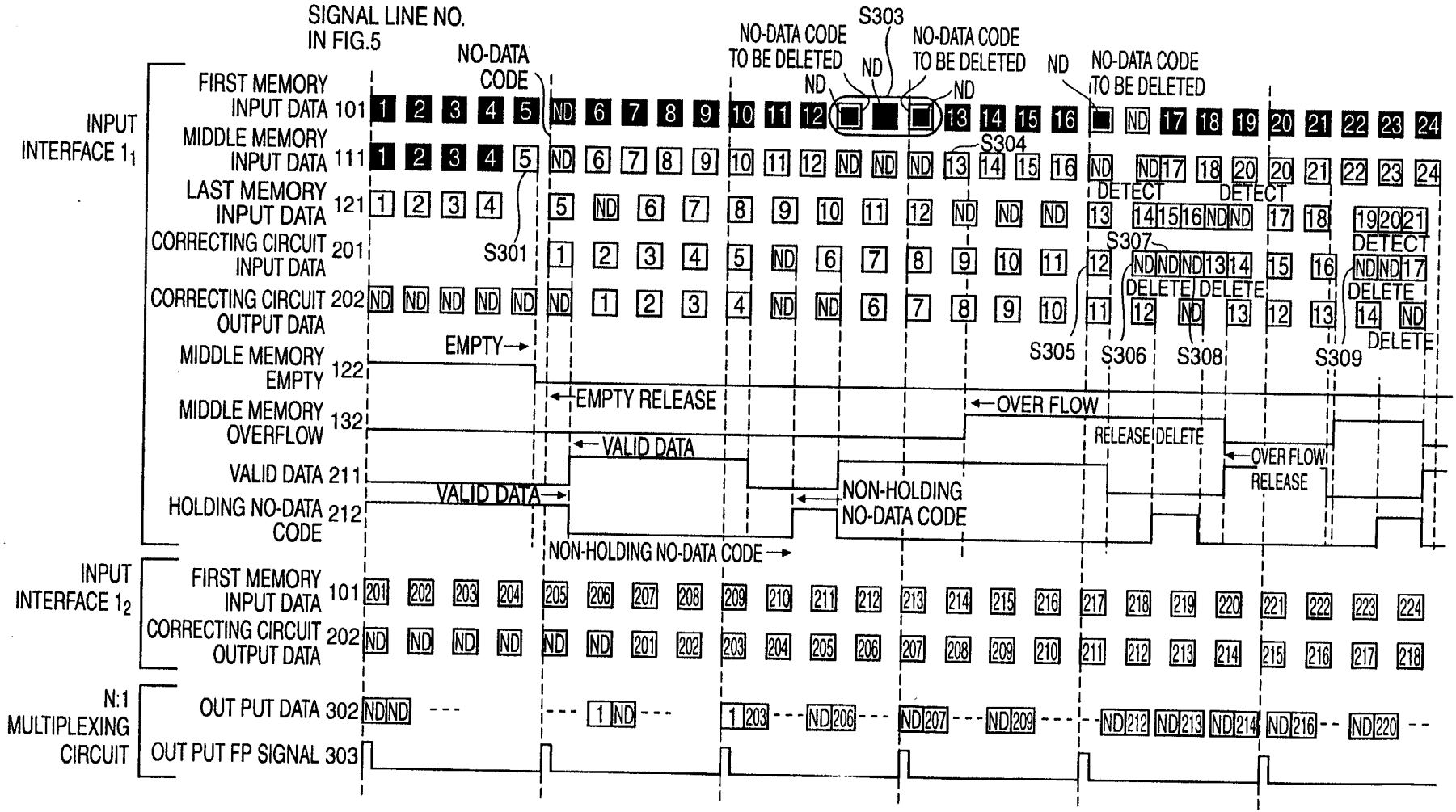

FIG.14

INPUT DATA	1	2	3	4	5	IC	6	7	8	9	10	11	12	(IC)	IC	(IC)	13	14	15	16
FIRST FIFO MEMORY																	S303	S304		
MIDDLE FIFO MEMORY				S301								11	12	(IC)	IC	(IC)	13	14	15	16
					(5)	IC	6	7	8	9	10	10	11	12	(IC)	IC	(IC)	13	14	15
							IC	6	7	8	9	9	10	11	12	(IC)	IC	IC	(IC)	14
LAST FIFO MEMORY	1	2 1	3 2 1	4 3 2 1	4 3 2 1	5 4 3 2	5 4 3 2	IC 5 4 3	6 IC 5 4	7 6 IC 5	8 7 6 IC	8 7 6 IC	9 8 7 6	10 9 8 7	11 10 9 8	12 11 10 9	12 11 10 9	(IC) 12 11 10	IC (IC) 12 11	(IC) IC (IC) 12
CIRCUIT INPUT	0		0	0	0	1		2	3	4	(5)		IC	6	7	8		9	10	11
CIRCUIT BUFFER	0	0	0	0	0	0	1	1	2	3	4	5	5	IC	6	7	8	8	9	10
CIRCUIT OUTPUT	0		0	0	0	0		1	2	3	4		5	IC	6	7		8	9	10
												S302								
EMPTY	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
OVERFLOW	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
VALID DATA	0	0	0	0	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1	1
HOLDING NO-DATA CODE	1	1	1	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0

INPUT DATA	(IC)	IC			17		18			19	20	21		22		23			24
FIRST FIFO MEMORY		IC																	
MIDDLE FIFO MEMORY	(IC) 16 15 14	(IC) 16 15 14	IC (IC) 16 15	IC (IC) 16	17 IC (IC) 16	17 IC (IC)	18 17 IC (IC)	18 17 IC	18	19 18 17	20 19 18	21 20 19 18	21 20 19	22 21 20 19	22 21 20	23 22 21 20	23 22 21	23 22	24 23 22
LAST FIFO MEMORY	13 (IC) IC (IC)	13 (IC) IC (IC)	14 13 (IC) IC	15 14 13 (IC)	15 14 13 (IC)	16 15 14 13	16 15 14 13	(IC) 16 15 14	IC (IC) 16 15	IC (IC) 16 15	17 IC (IC) 16	17 IC (IC) 16	18 17 IC (IC)	18 17 IC (IC)	19 18 17 IC	19 18 17 IC	20 19 18 17	21 20 19 18	21 20 19 18
CIRCUIT INPUT	12		(IC)	(IC)		(IC)		13	14		15		16		(IC)		IC	17	
CIRCUIT BUFFER	11	(12)	12	(IC)	IC	IC	(IC)	(IC)	13	14	14	15	15	16	16	(IC)	(IC)	IC	17
CIRCUIT OUTPUT	11		12			IC			13		14		15		16			IC	
				DL				DL									DL		
EMPTY	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
OVERFLOW	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0
VALID DATA	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0
HOLDING NO-DATA CODE	0	0	0	(1)	1	1	(1)	(1)	0	0	0	0	0	0	0	(1)	(1)	1	0

S309

S305 S306 S307 S308